Si5017

OC-48/STM-16 SONET/SDH CDR IC WITH LIMITING AMPLIFIER

Features

High-speed clock and data recovery device with integrated limiting amplifier:

- Supports OC-48/STM-16 and 2.7 Gbps FEC
- DSPLL® technology
- Jitter generation 3.0 mUI_{rms} (typ)
- Small footprint: 5 x 5 mm
- Loss-of-signal level alarm
- Data slicing level control
- 10 mV_{PP} differential sensitivity
- 3.3 V supply
- Reference and reference-less operation supported



Ordering Information:

See page 22.

Applications

- SONET/SDH/ATM routers
- Add/drop multiplexers
- Digital cross connects
- Board level serial links
- SONET/SDH test equipment
- Optical transceiver modules
- SONET/SDH regenerators

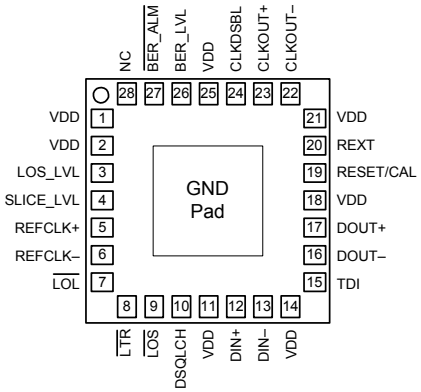
Description

The Si5017 is a fully-integrated, high-performance limiting amplifier (LA) and clock and data recovery (CDR) IC for high-speed serial communication systems. It derives timing information and data from a serial input at OC-48 and STM-16 rates. Support for 2.7 Gbps data streams is also provided for OC-48/STM-16 applications that employ forward error correction (FEC). Use of an external reference clock is optional. Silicon Laboratories DSPLL® technology eliminates sensitive noise entry points, thus making the PLL less susceptible to board-level interaction and helping to ensure optimal jitter performance.

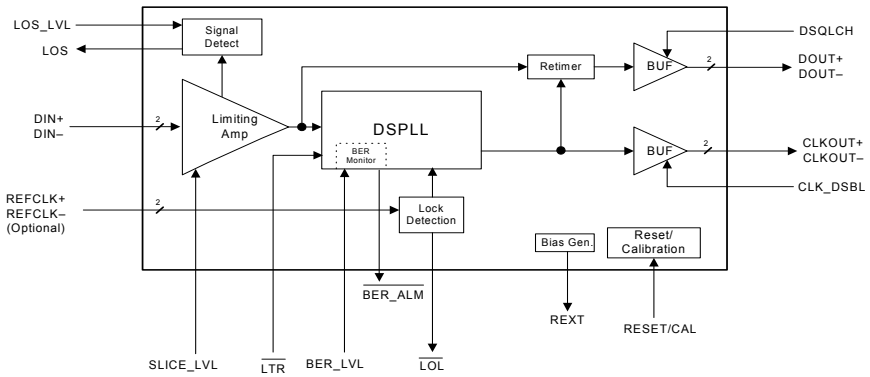
The Si5017 represents a new standard in low jitter, low power, small size, and integration for high-speed LA/CDRs. It operates from a 3.3 V supply over the industrial temperature range (–40 to 85 °C).

Pin Assignments

Si5017



Functional Block Diagram



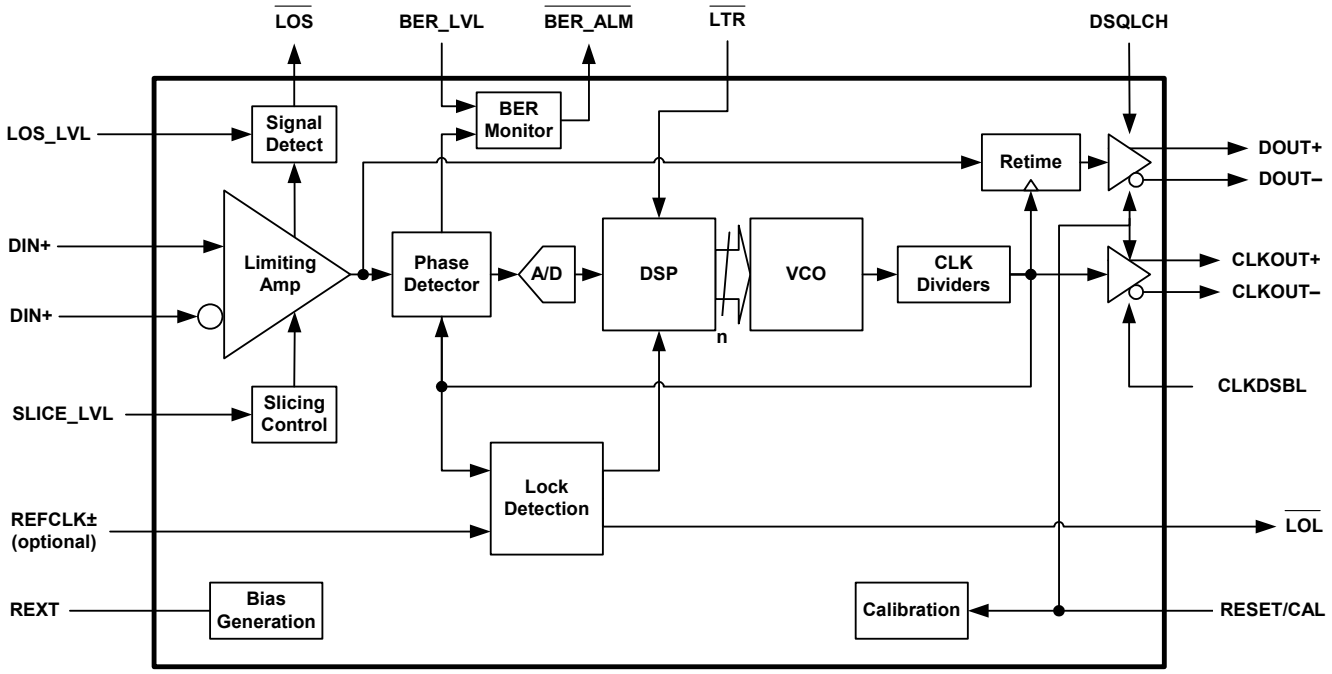
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1. Detailed Block Diagram

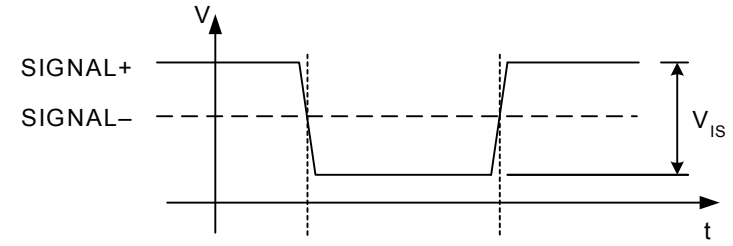


2. Electrical Specifications

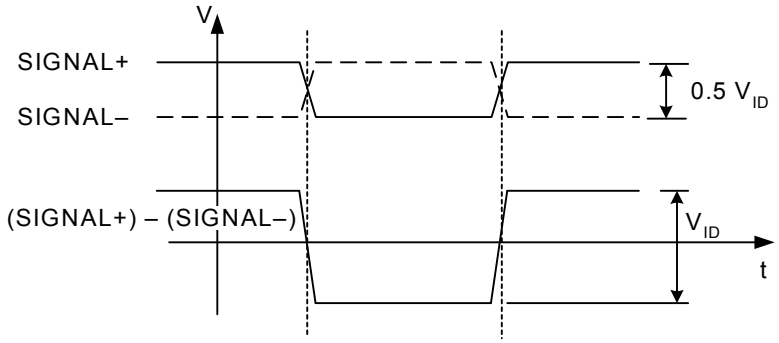
Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min[1]	Typ	Max[1]	Unit
Ambient Temperature	T_A		–40	25	85	°C
Si5017 Supply Voltage[2]	V_{DD}		3.135	3.3	3.465	V

Notes:
1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
2. The Si5017 specifications are guaranteed when using the recommended application circuit (including component tolerance) of the "3. Typical Application Schematic" on page 11.



A. Operation with Single-Ended Inputs



B. Operation with Differential Inputs and Outputs

Figure 1. Differential Voltage Measurement (DIN, REFCLK, DOUT, CLKOUT)

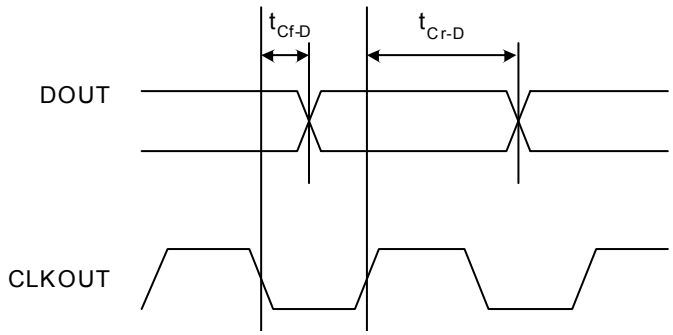


Figure 2. Clock to Data Timing

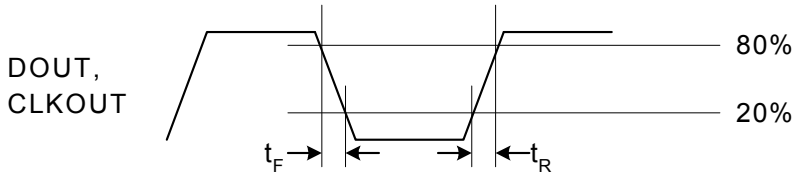


Figure 3. DOUT and CLKOUT Rise/Fall Times

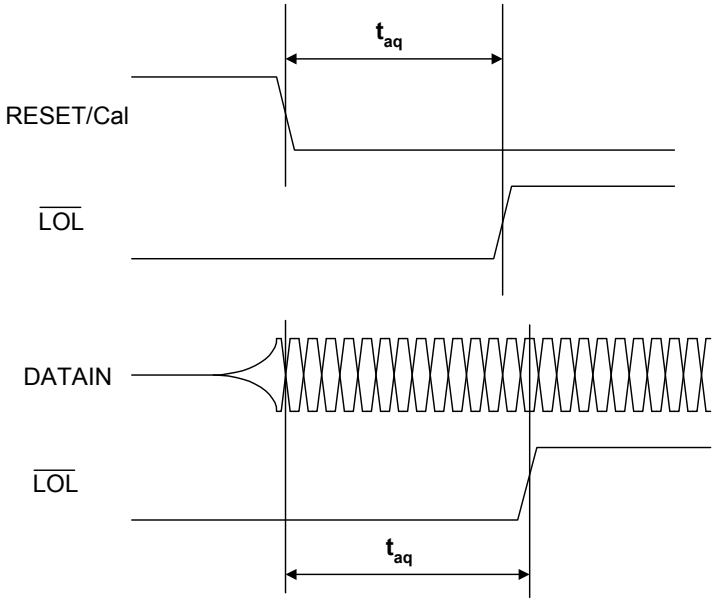


Figure 4. PLL Acquisition Time

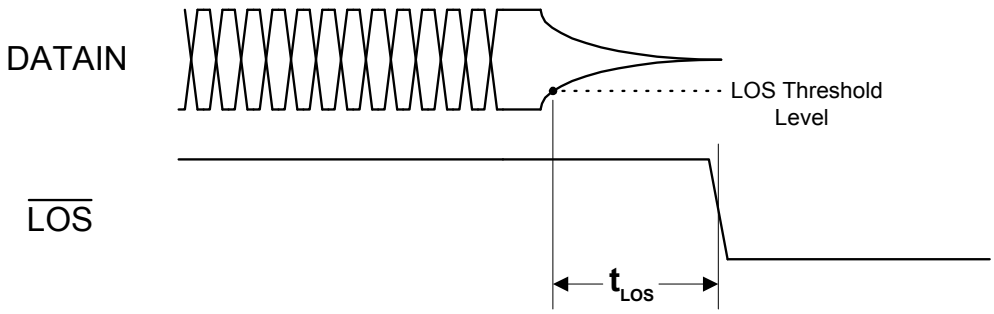


Figure 5. LOS Response Time

Table 2. DC Characteristics
(V_{DD} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current[1] FEC (2.7 Gbps) OC-48	I_{DD}		 — —	 173 170	 184 180	mA
Power Dissipation FEC (2.7 Gbps) OC-48	P_D		 — —	 571 561	 637 623	mW
Common Mode Input Voltage (DIN)[2]	V_{ICM}	See Figure 11	1.30	1.50	1.62	V
Common Mode Input Voltage (REFCLK)[2]	V_{ICM}	See Figure 10	1.90	2.10	2.30	V
DIN Single-ended Input Voltage Swing[2]	V_{IS}	See Figure 1A	10	—	500	mV
DIN Differential Input Voltage Swing[2]	V_{ID}	See Figure 1B	10	—	1000	mV
REFCLK Single-ended Input Voltage Swing[2]	V_{IS}	See Figure 1A	200	—	750	mV
REFCLK Differential Input Voltage Swing[2]	V_{ID}	See Figure 1B	200	—	1500	mV
Input Impedance (DIN)	R_{IN}	Line-to-Line	84	100	116	Ω
Differential Output Voltage Swing (DOUT)	V_{OD}	100 Ω Load Line-to-Line	700	800	1000	mV_{PP}
Differential Output Voltage Swing (CLKOUT)	V_{OD}	100 Ω Load Line-to-Line	700	800	1100	mV_{PP}
Output Common Mode Voltage (DOUT)	V_{OCM}	100 Ω Load Line-to-Line	1.6	1.95	2.35	V
Output Common Mode Voltage (CLKOUT)	V_{OCM}	100 Ω Load Line-to-Line	1.6	1.80	2.35	V
Output Impedance (DOUT,CLKOUT)	R_{OUT}	Single-ended	84	100	116	Ω
Input Voltage Low (LVTTL Inputs)	V_{IL}		—	—	.8	V
Input Voltage High (LVTTL Inputs)	V_{IH}		2.0	—	—	V
Input Low Current (LVTTL Inputs)	I_{IL}		—	—	10	µA
Input High Current (LVTTL Inputs)	I_{IH}		—	—	10	µA
Input Impedance (LVTTL Inputs)	R_{IN}		9	—	—	kΩ
LOS_LVL, BER_LVL, SLICE_LVL Input Impedance	R_{IN}		50	100	125	kΩ
Output Voltage Low (LVTTL Outputs)	V_{OL}	I_O = 2 mA	—	—	0.4	V
Output Voltage High (LVTTL Outputs)	V_{OH}	I_O = 2 mA	2.0	—	—	V

Notes:
1. No load on LVTTL outputs.
2. These inputs may be driven differentially or single-endedly. When driven single-endedly, the unused input must be ac coupled to ground.

Table 3. AC Characteristics (Clock and Data)
(V_{DD} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Clock Rate	f_{CLK}		2.4	—	2.7	GHz
Output Clock Rise Time	t_R	Figure 3	—	70	90	ps
Output Clock Fall Time	t_F	Figure 3	—	70	90	ps
Output Clock Duty Cycle			48	50	52	% of UI
Output Data Rise Time	t_R	Figure 3	—	80	110	ps
Output Data Fall Time	t_F	Figure 3	—	80	110	ps
Clock to Data Delay FEC (2.7 Gbps) OC-48	t_{Cr-D}	Figure 2	 190 190	 230 230	 265 265	ps
Clock to Data Delay FEC (2.7 Gbps) OC-48	t_{Cf-D}	Figure 2	 –70 –60	 –40 –30	 –10 0	ps
Input Return Loss		100 kHz–1.5 GHz 1.5 GHz–4.0 GHz	–15 –10	— —	— —	dB dB
Slicing Level Offset (relative to the internally set input common mode voltage)	V_{SLICE}	SLICE_LVL = 750 mV to 2.25 V	See Figure 8 on page 14.			
Loss-of-Signal Range* (peak-to-peak differential)	V_{LOS}	LOS_LVL = 1.50 to 2.50 V	0	—	40	mV
Loss-of-Signal Response Time	t_{LOS}	Figure 5	8	20	25	µs

***Note:** Adjustment voltage is calculated as follows: V_{LOS} = (LOS_LVL – 1.50)/25.

Table 4. AC Characteristics (PLL Characteristics)
(V_{DD} =3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Jitter Tolerance (OC-48)*	$J_{TOL(PP)}$	f = 600 Hz	40	—	—	UI_{PP}
		f = 6000 Hz	4	—	—	UI_{PP}
		f = 100 kHz	3	—	—	UI_{PP}
		f = 1 MHz	0.3	—	—	UI_{PP}
RMS Jitter Generation*	$J_{GEN(rms)}$	with no jitter on serial data	—	3.0	5.0	mUI
Peak-to-Peak Jitter Generation*	$J_{GEN(PP)}$	with no jitter on serial data	—	25	55	mUI
Jitter Transfer Bandwidth*	J_{BW}	OC-48	—	—	2.0	MHz
Jitter Transfer Peaking*	J_P		—	0.03	0.1	dB
Acquisition Time (Reference clock applied)	T_{AQ}	After falling edge of RESET/CAL	—	1.6	2.2	ms
		From the return of valid data	20	100	500	µs
Acquisition Time (Reference-less operation)	T_{AQ}	After falling edge of RESET/CAL	—	2.0	5.5	ms
		From the return of valid data	1.5	2.5	5.5	ms
Reference Clock Range See Table 7 on page 13.		f_{CLK} / 16 f_{CLK} / 32 f_{CLK} / 128	— — —	155.52 77.76 19.44	— — —	MHz
Input Reference Clock Frequency Tolerance	C_{TOL}		–500	—	+500	ppm
Frequency Difference at which Receive PLL goes out of Lock (REFCLK compared to the divided down VCO clock)			—	±650	—	ppm

***Note:** As defined in Bellcore specifications: GR-253-CORE, Issue 3, September 2000. Using PRBS 2^{23} – 1 data pattern.

Table 5. Absolute Maximum Ratings

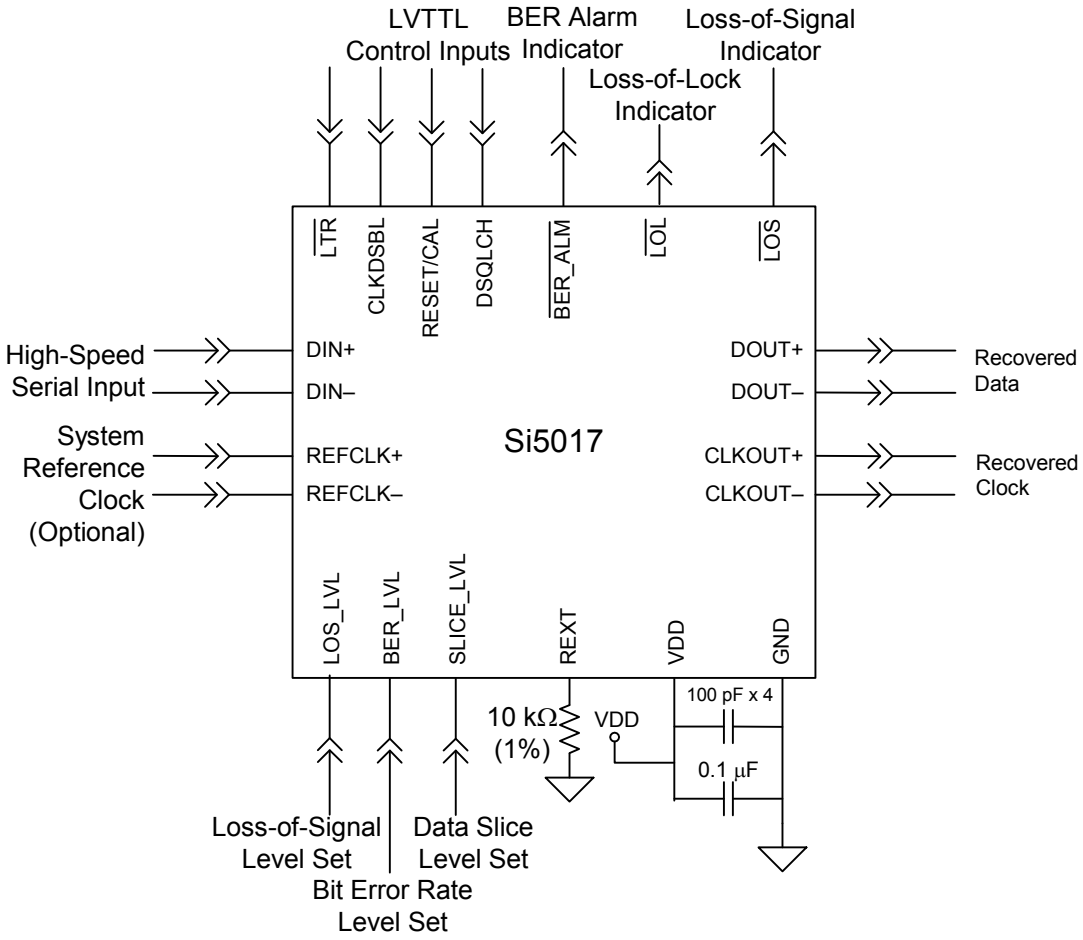
Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 3.5	V
LVTTL Input Voltage	V_{DIG}	–0.3 to 3.6	V
Differential Input Voltages	V_{DIF}	–0.3 to (V_{DD}+ 0.3)	V
Maximum Current any output PIN		±50	mA
Operating Junction Temperature	T_{JCT}	–55 to 150	°C
Storage Temperature Range	T_{STG}	–55 to 150	°C
ESD HBM Tolerance (100 pf, 1.5 kΩ)		1	kV

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	φ_{JA}	Still Air	38	°C/W

3. Typical Application Schematic



4. Functional Description

The Si5017 integrates a high-speed limiting amplifier with a CDR unit that operates between 2.4 and 2.7 Gbps. No external reference clock is required for clock and data recovery. The limiting amplifier magnifies very low-level input data signals so accurate clock and data recovery can be performed. The CDR uses Silicon Laboratories DSPLL® technology to recover a clock synchronous to the input data stream. The recovered clock retimes the incoming data, and both are output synchronously via current-mode logic (CML) drivers. Silicon Laboratories' DSPLL technology ensures superior jitter performance while eliminating the need for external loop filter components found in traditional phase-locked loop (PLL) implementations.

The limiting amplifier includes a control input for adjusting the data slicing level and provides a loss-of-signal level alarm output. The CDR includes a bit-error-rate performance monitor which signals a high bit-error-rate condition (associated with excessive incoming jitter) relative to an externally adjustable bit-error-rate threshold.

The optional reference clock minimizes the CDR acquisition time and provides a stable reference for maintaining the output clock when locking to reference is desired.

4.1. Limiting Amplifier

The limiting amplifier accepts the low-level signal output from a transimpedance amplifier (TIA). The low-level signal is amplified to a usable level for the CDR unit. The minimum input swing requirement is specified in Table 2. Larger input amplitudes (up to the maximum input swing specified in Table 2) are accommodated without degradation of performance. The limiting amplifier ensures optimal data slicing by using a digital dc offset cancellation technique to remove any dc bias introduced by the amplification stage.

4.2. DSPLL®

The Si5017 PLL structure (shown in the "1. Detailed Block Diagram" on page 4) utilizes Silicon Laboratories' DSPLL technology to maintain superior jitter performance while eliminating the need for external loop filter components found in traditional PLL implementations. This is achieved using a digital signal processing (DSP) algorithm to replace the loop filter commonly found in analog PLL designs. This algorithm processes the phase detector error term and generates a digital control value to adjust the frequency of the voltage-controlled oscillator (VCO). This technology enables CDR with far less jitter than is generated using traditional methods, and it eliminates performance degradation caused by external component aging. In addition, because external loop filter components are not required, sensitive noise entry points are eliminated, thus making the DSPLL less susceptible to board-level noise sources and making SONET/SDH jitter compliance easier to attain in the application.

4.3. Operation Without an External Reference

The Si5017 can perform clock and data recovery without an external reference clock. Tying the REFCLK+ input to VDD and the REFCLK– input to GND configures the device to operate without an external reference clock. Clock recovery is achieved by monitoring the timing quality of the incoming data relative to the VCO frequency. Lock is maintained by continuously monitoring the incoming data timing quality and adjusting the VCO accordingly. Details of the lock detection and the lock-to-reference functions while in this mode are described in their respective sections below.

Note: Without an external reference the acquisition of data is dependent solely on the data itself and typically requires more time to acquire lock than when a reference is applied.

4.4. Operation With an External Reference

The Si5017 can also perform clock and data recovery with an external reference. The device's optional external reference clock centers the DSPLL, minimizes the acquisition time, and maintains a stable output clock (CLKOUT) when lock-to-reference ($\overline{\text{LTR}}$) is asserted.

When the reference clock is present, the Si5017 uses the reference clock to center the VCO output frequency so that clock and data are recovered from the input data stream. The device self configures for operation with one of three reference clock frequencies. This eliminates the need to externally configure the device to operate with a particular reference clock.

The reference clock centers the VCO for a nominal output between 2.5 and 2.7 GHz. The VCO frequency is centered at 16, 32, or 128 times the reference clock frequency. Detection circuitry continuously monitors the reference clock input to determine whether the device should be configured for a reference clock that is 1/16, 1/32, or 1/128 the nominal VCO output. Approximate reference clock frequencies for some target applications are given in Table 7.

Table 7. Typical REFCLK Frequencies

SONET/SDH	OC-48 with 15/14 FEC	Ratio of VCO to REFCLK
19.44 MHz	20.83 MHz	128
77.76 MHz	83.31 MHz	32
155.52 MHz	166.63 MHz	16

4.5. Lock Detect

The Si5017 provides lock-detect circuitry that indicates whether the PLL has achieved frequency lock with the incoming data. The operation of the lock-detector depends on the reference clock option used.

When an external reference clock is provided, the circuit compares the frequency of a divided-down version of the recovered clock with the frequency of the applied reference clock (REFCLK). If the recovered clock frequency deviates from that of the reference clock by the amount specified in Table 4 on page 9, the PLL is declared out of lock, and the loss-of-lock ($\overline{LOL}$) pin is asserted. In this state, the PLL will periodically try to reacquire lock with the incoming data stream. During reacquisition, the recovered clock frequency (CLKOUT) drifts over a ±600 ppm range relative to the applied reference clock and the LOL output alarm may toggle until the PLL has reacquired frequency lock. Due to the low noise and stability of the DSPLL, there is the possibility that the PLL will not drift enough to render an out-of-lock condition, even if the data is removed from inputs.

In applications requiring a more stable output clock during out-of-lock conditions, the lock-to-reference ($\overline{LTR}$) input can be used to force the PLL to lock to the externally supplied reference.

In the absence of an external reference, the lock detect circuitry uses a data quality measure to determine when frequency lock has been lost with the incoming data stream. During reacquisition, CLKOUT may vary by approximately ±10% from the nominal data rate.

4.6. Lock-to-Reference

The $\overline{LTR}$ input is used to force a stable output clock when an alarm condition, like LOS, exists. In typical applications, the $\overline{LOS}$ output is tied to the $\overline{LTR}$ input to force a stable output clock when the input data signal is lost. When $\overline{LTR}$ is asserted, the DSPLL is prevented from acquiring the data signal present on DIN. The operation of the $\overline{LTR}$ control input depends on which reference clocking mode is used.

When an external reference clock is present, assertion of $\overline{LTR}$ forces the DSPLL to lock CLKOUT to the provided reference. If no external reference clock is used, $\overline{LTR}$ forces the DSPLL to hold the digital frequency control input to the VCO at the last value. This produces a stable output clock as long as supply and temperature are constant.

4.7. Loss-of-Signal (LOS)

The Si5017 indicates a loss-of-signal condition on the $\overline{LOS}$ output pin when the input peak-to-peak signal level on DIN falls below an externally controlled threshold. The LOS threshold range is specified in Table 3 and is set by applying a voltage on the LOS_LVL pin. The graph in Figure 6 illustrates the LOS_LVL mapping to the LOS threshold. The $\overline{LOS}$ output is asserted when the input signal drops below the programmed peak-to-peak value. If desired, the $\overline{LOS}$ function may be disabled by grounding LOS_LVL or by adjusting LOS_LVL to be less than 1 V.

Note: The LOS circuit is designed to only work with pseudo-random, dc-balanced data.

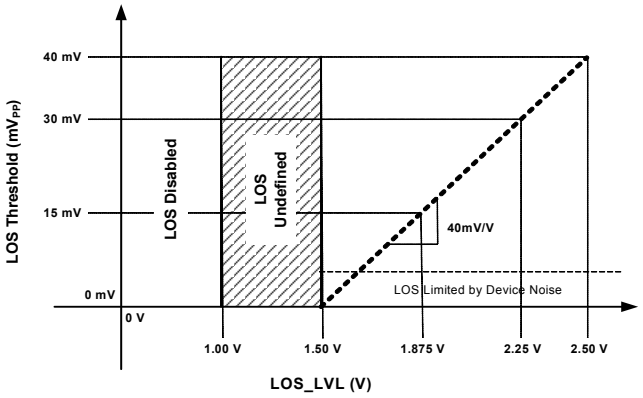


Figure 6. LOS_LVL Mapping

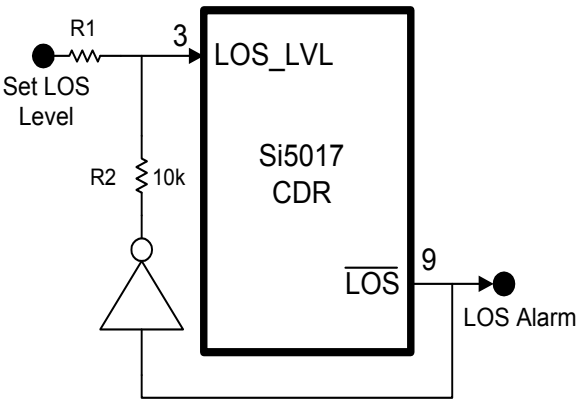


Figure 7. LOS Signal Hysteresis

In many applications it is desirable to produce a fixed amount of signal hysteresis for an alarm indicator such as LOS, since a marginal data input signal could cause intermittent toggling, leading to false alarm status. When it is anticipated that very low-level DIN signals will be encountered, the introduction of an adequate amount of LOS hysteresis is recommended to minimize any undesirable LOS signal toggling. Figure 7 illustrates a simple circuit that may be used to set a fixed level of LOS signal hysteresis for the Si5017 CDR. The value of R1 may be chosen to provide a range of hysteresis from 3 to 8 dB where a nominal value of 800 Ω adjusts the hysteresis level to approximately 6 dB. Use a value of 500 Ω or 1000 Ω for R1 to provide 3 dB or 8 dB of hysteresis, respectively.

Hysteresis is defined as the ratio of the LOS deassert level (LOSD) and the LOS assert level (LOSA). The hysteresis in decibels is calculated as 20log(LOSD/LOSA).

4.8. Bit-Error-Rate (BER) Detection

The Si5017 uses a proprietary Silicon Laboratories algorithm to generate a bit-error-rate (BER) alarm on the BER_ALM pin if the observed BER is greater than a user programmable threshold. Bit error detection relies on the input data edge timing; edges occurring outside of the expected event window are counted as bit errors. The BER threshold is programmed by applying a voltage to the BER_LVL pin between 500 mV and 2.25 V corresponding to a BER of approximately 10–10 and 10–6, respectively. The voltage present on BER_LVL maps to the BER as follows: log10(BER) = (4 x BER_LVL) – 13. (BER_LVL is in volts; BER is in bits per second.).

4.9. Data Slicing Level

The Si5017 provides the ability to externally adjust the slicing level for applications that require bit-error-rate (BER) optimization. Adjustments in slicing level of ±25 mV (typical, relative to the internally set input common mode voltage) are supported. The slicing level is set by applying a voltage between 0.75 and 2.25 V to the SLICE_LVL input. See Figure 8 for the operation levels of the slice circuit.

When SLICE_LVL is driven below 500 mV, the slicing level adjustment is disabled, and the slicing level is set to the cross-point of the differential input signal.

Note: The slice circuit is designed to only work with pseudo-random, dc-balanced data.

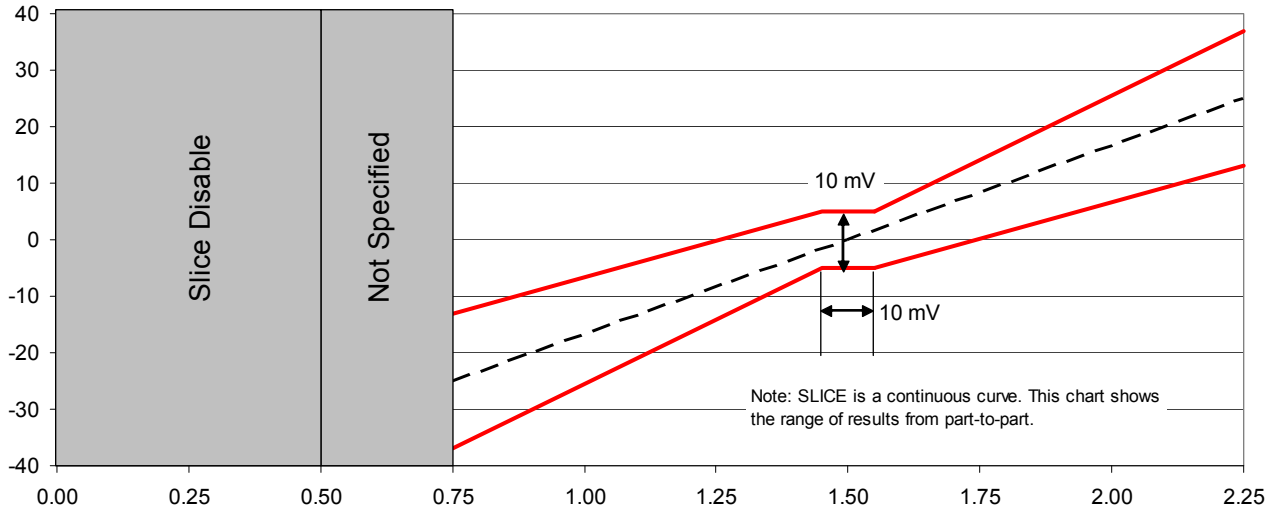


Figure 8. Si5017 OC-48 Slice Specification

4.10. PLL Performance

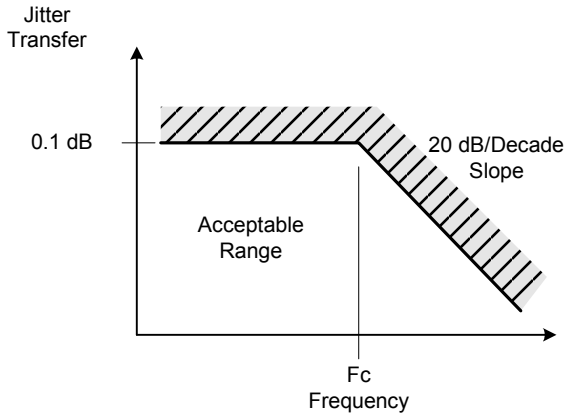
The PLL implementation used in the Si5017 is fully compliant with the jitter specifications proposed for SONET/SDH equipment by Bellcore GR-253-CORE, Issue 3, September 2000 and ITU-T G.958.

4.10.1. Jitter Tolerance

The Si5017's tolerance to input jitter exceeds that of the Bellcore/ITU mask shown in Figure 8. This mask defines the level of peak-to-peak sinusoid jitter that must be tolerated when applied to the differential data input of the device.

4.10.2. Jitter Transfer

The Si5017 exceeds all relevant Bellcore/ITU specifications related to SONET/SDH jitter transfer. Jitter transfer is defined as the ratio of output signal jitter to input signal jitter as a function of jitter frequency. These measurements are made with an input test signal that is degraded with sinusoidal jitter whose magnitude is defined by the mask in Figure 9.



SONET Data Rate	Fc (kHz)
OC-48	2000

Figure 9. Jitter Transfer Specification

4.10.3. Jitter Generation

The Si5017 exceeds all relevant specifications for jitter generation proposed for SONET/SDH equipment. The jitter generation specification defines the amount of jitter that may be present on the recovered clock and data outputs when a jitter free input signal is provided. The Si5017 typically generates less than 3.0 mUI_{rms} of jitter when presented with jitter-free input data.

4.11. RESET/DSPLL Calibration

The Si5017 achieves optimal jitter performance by automatically calibrating the loop gain parameters within the DSPLL on powerup. Calibration may also be initiated by a high-to-low transition on the RESET/CAL pin. The RESET/CAL pin must be held high for at least 1 μs. When RESET/CAL is released (set to low) the digital logic resets to a known initial condition, recalibrates the DSPLL, and begins to lock to the incoming data stream. For a valid reset to occur when using Reference mode, a proper, external reference clock frequency must be applied as specified in Table 7.

4.12. Clock Disable

The Si5017 provides a clock disable pin (CLK_DSBL) that is used to disable the recovered clock output (CLKOUT). When the CLK_DSBL pin is asserted, the positive and negative terminals of CLKOUT are tied to VDD through 100 Ω on-chip resistors.

4.13. Data Squelch

The Si5017 provides a data squelching pin (DSQLCH) that is used to set the recovered data output (DOUT) to binary zero. When the DSQLCH pin is asserted, the DOUT+ signal is held low and the DOUT– signal is held high. This pin can be is used to squelch corrupt data during LOS and LOL situations. Care must be taken when ac coupling these outputs; a long string of zeros or ones will not be held through ac coupling capacitors.

4.14. Device Grounding

The Si5017 uses the GND pad on the bottom of the 28-pin micro leaded package (QFN) for device ground. This pad should be connected directly to the analog supply ground. See Figure 15 on page 19 and Figure 16 on page 23 for the ground (GND) pad location.

4.15. Bias Generation Circuitry

The Si5017 makes use of an external resistor to set internal bias currents. The external resistor allows precise generation of bias currents which significantly reduces power consumption versus traditional implementations that use an internal resistor. The bias generation circuitry requires a 10 kΩ (1%) resistor connected between REXT and GND.

4.16. Voltage Regulator

The Si5017 operates from a 3.3 V external supply voltage. Internally the device operates from a 2.5 V supply. The Si5017 regulates 2.5 V internally down from the external 3.3 V supply.

In addition to supporting 3.3 V systems, the on-chip linear regulator offers better power supply noise rejection versus a direct 2.5 V supply.

4.17. Differential Input Circuitry

The Si5017 provides differential inputs for both the high-speed data (DIN) and the reference clock (REFCLK) inputs. An example termination for these inputs is shown in Figures 10 and 11, respectively. In applications where direct dc coupling is possible, the 0.1 µF capacitors may be omitted. (LOS operation is only guaranteed when ac coupled.) The data input limiting amplifier requires an input signal with a differential peak-to-peak voltage as specified in Table 2 on page 7 to ensure a BER of at least 10^{-12}. The REFCLK input differential peak-to-peak voltage requirement is also specified in Table 2.

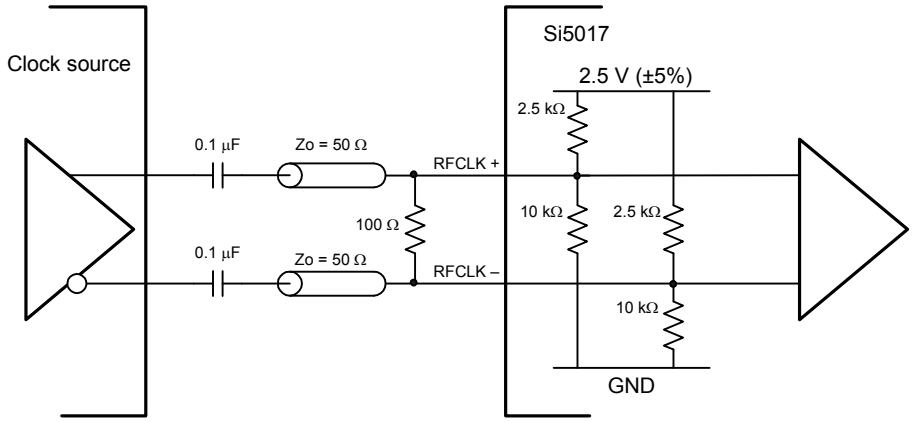


Figure 10. Input Termination for REFCLK (ac coupled)

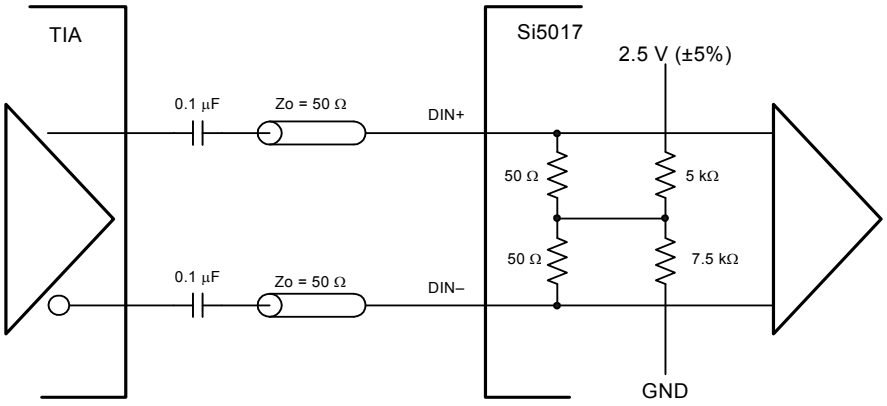


Figure 11. Input Termination for DIN (ac coupled)

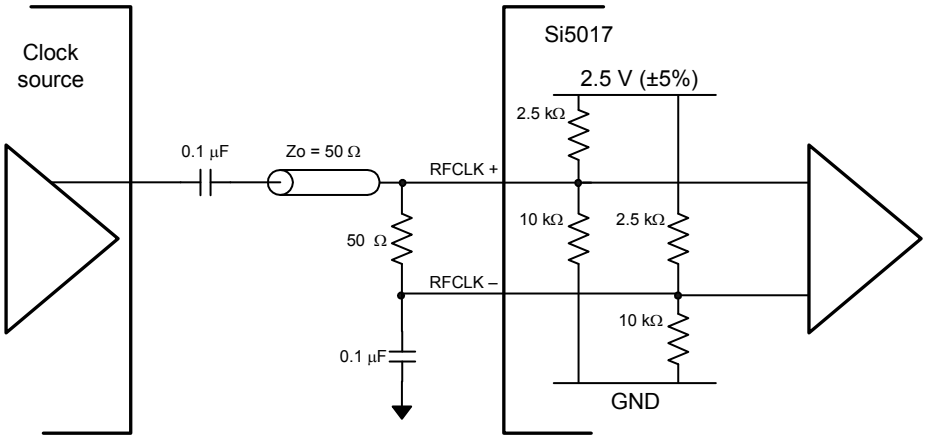


Figure 12. Single-Ended Input Termination for REFCLK (ac coupled)

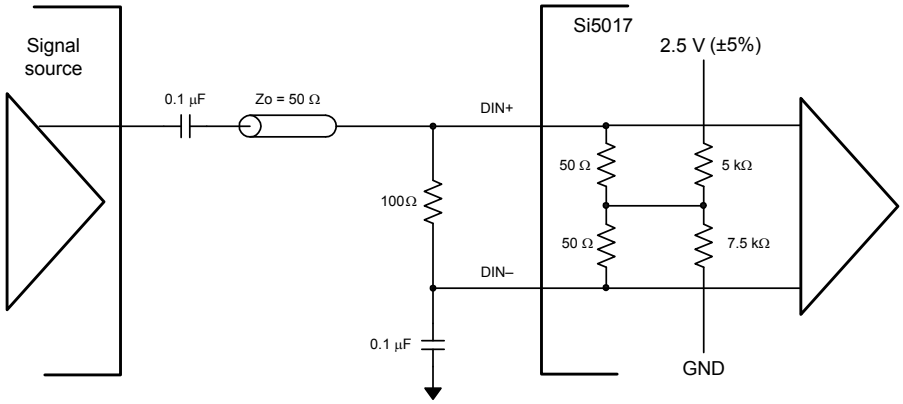


Figure 13. Single-Ended Input Termination for DIN (ac coupled)

4.18. Differential Output Circuitry

The Si5017 utilizes a CML architecture to output both the recovered clock (CLKOUT) and data (DOUT). An example of output termination with ac coupling is shown in Figure 14. In applications in which direct dc coupling is possible, the 0.1 μF capacitors may be omitted. The differential peak-to-peak voltage swing of the CML architecture is specified in Table 2 on page 7.

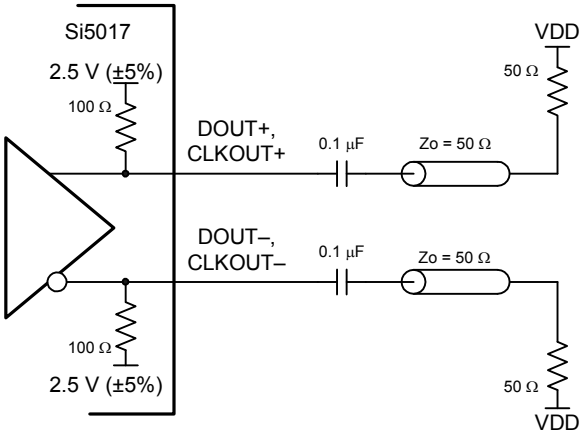


Figure 14. Output Termination for DOUT and CLKOUT (ac coupled)

5. Pin Descriptions: Si5017

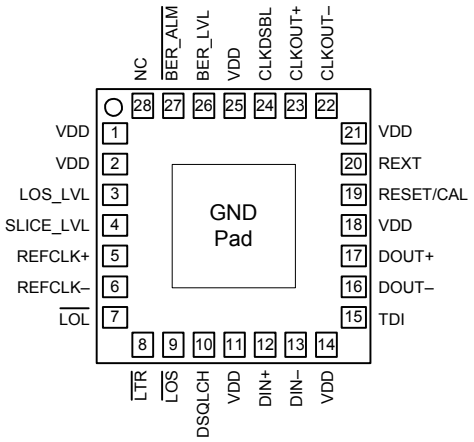


Figure 15. Si5017 Pin Configuration

Table 8. Si5017 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
1,2,11,14,18, 21,25	VDD		3.3 V	**Supply Voltage.** Nominally 3.3 V.
3	LOS_LVL	I		**LOS Level Control.** The LOS threshold is set by the input voltage level applied to this pin. Figure 6 on page 13 shows the input setting to output threshold mapping. LOS is disabled when the voltage applied is less than 1 V.
4	SLICE_LVL	I		**Slicing Level Control.** The slicing threshold level is set by applying a voltage to this pin as described in the Slicing Level section of the data sheet. If this pin is tied to GND, slicing level adjustment is disabled, and the slicing level is set to the midpoint of the differential input signal on DIN. Slicing level becomes active when the voltage applied to the pin is greater than 500 mV.
5 6	REFCLK+ REFCLK–	I	See Table 2	**Differential Reference Clock (Optional).** When present, the reference clock sets the center operating frequency of the DSPLL for clock and data recovery. Tie REFCLK+ to VDD and REFCLK– to GND to operate without an external reference clock. See Table 7 on page 13 for typical reference clock frequencies.

Table 8. Si5017 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
7	$\overline{\text{LOL}}$	O	LVTTL	**Loss-of-Lock.** This output is driven low when the recovered clock frequency deviates from the reference clock by the amount specified in Table 4 on page 9. If no external reference is supplied, this signal will be active when the internal PLL is no longer locked to the incoming data.
8	$\overline{\text{LTR}}$	I	LVTTL	**Lock-to-Reference.** When this pin is low, the DSPLL disregards the data inputs. If an external reference is supplied, the output clock locks to the supplied reference. If no external reference is used, the DSPLL locks the control loop until $\overline{\text{LTR}}$ is released. **Note:** This input has a weak internal pullup.
9	$\overline{\text{LOS}}$	O	LVTTL	**Loss-of-Signal.** This output pin is driven low when the input signal is below the threshold set via LOS_LVL. (LOS operation is guaranteed only when ac coupling is used on the DIN inputs.)
10	DSQLCH		LVTTL	**Data Squelch.** When driven high, this pin forces the data present on DOUT+ to zero and DOUT– to one. For normal operation, this pin should be low. DSQLCH may be used during LOS/LOL conditions to prevent random data from being presented to the system. **Note:** This input has a weak internal pulldown.
12 13	DIN+ DIN–	I	See Table 2	**Differential Data Input.** Clock and data are recovered from the differential signal present on these pins. AC coupling is recommended.
15	GND		GND	**Production Test Input.** This pin is used during production testing and *must* be tied to GND for normal operation.
16 17	DOUT– DOUT+	O	CML	**Differential Data Output.** The data output signal is a retimed version of the data recovered from the signal present on DIN.
19	RESET/CAL	I	LVTTL	**Reset/Calibrate.** Driving this input high for at least 1 µs will reset internal device circuitry. A high to low transition on this pin will force a DSPLL calibration. For normal operation, drive this pin low. **Note:** This input has a weak internal pulldown.
20	REXT			**External Bias Resistor.** This resistor is used to establish internal bias currents within the device. This pin must be connected to GND through a 10 kΩ (1%) resistor.

Table 8. Si5017 Pin Descriptions (Continued)

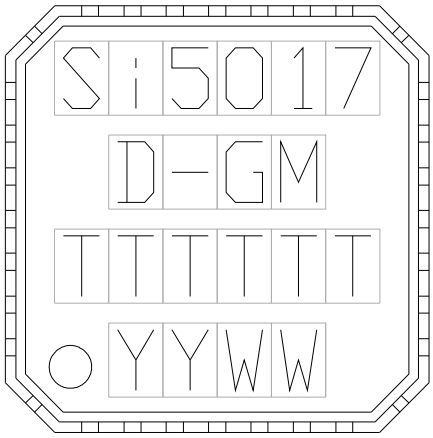
Pin #	Pin Name	I/O	Signal Level	Description
22 23	CLKOUT– CLKOUT+	O	CML	**Differential Clock Output.** The output clock is recovered from the data signal present on DIN except when LTR is asserted or the LOL state has been entered.
24	CLKDSBL	I	LVTTL	**Clock Disable.** When this input is high, the CLKOUT output drivers are disabled. For normal operation, this pin should be low. **Note:** This input has a weak internal pulldown.
26	BER_LVL	I		**Bit Error Rate Level Control.** The BER threshold level is set by applying a voltage to this pin. When the BER exceeds the programmed threshold, BER_ALM is driven low. If this pin is tied to GND, BER_ALM is disabled.
27	BER_ALM	O	LVTTL	**Bit Error Rate Alarm.** This pin will be driven low to indicate that the BER threshold set by BER_LVL has been exceeded. There is no hysteresis.
28	NC			**No Connect.** Leave this pin disconnected.
GND Pad	GND		GND	**Supply Ground.** Nominally 0.0 V. The GND pad found on the bottom of the 28-lead QFN (see Figure 16 on page 23) **must be connected** directly to supply ground. Minimize the ground path inductance for optimal performance.

6. Ordering Guide

Part Number	Package	Voltage	Pb-Free	Temperature
Si5017-X-GM	28-Lead QFN	3.3	Yes	–40 to 85 °C

1. “X” denotes product revision.
2. Add an “R” at the end of the device to denote tape and reel option; 2500 quantity per reel.
3. These devices use a NiPdAu pre-plated finish on the leads that is fully RoHS6 compliant while being fully compatible with both leaded and lead-free card assembly processes.

7. Top Mark



Part Number	Die Revision—Device Type	Assembly Date (YYWW)
Si5017	D-GM	YY = Year WW = Work week

8. Package Outline

Figure 16 illustrates the package details for the Si5017. Table 9 lists the values for the dimensions shown in the illustration. For a pad layout recommendation please contact Silicon Laboratories.

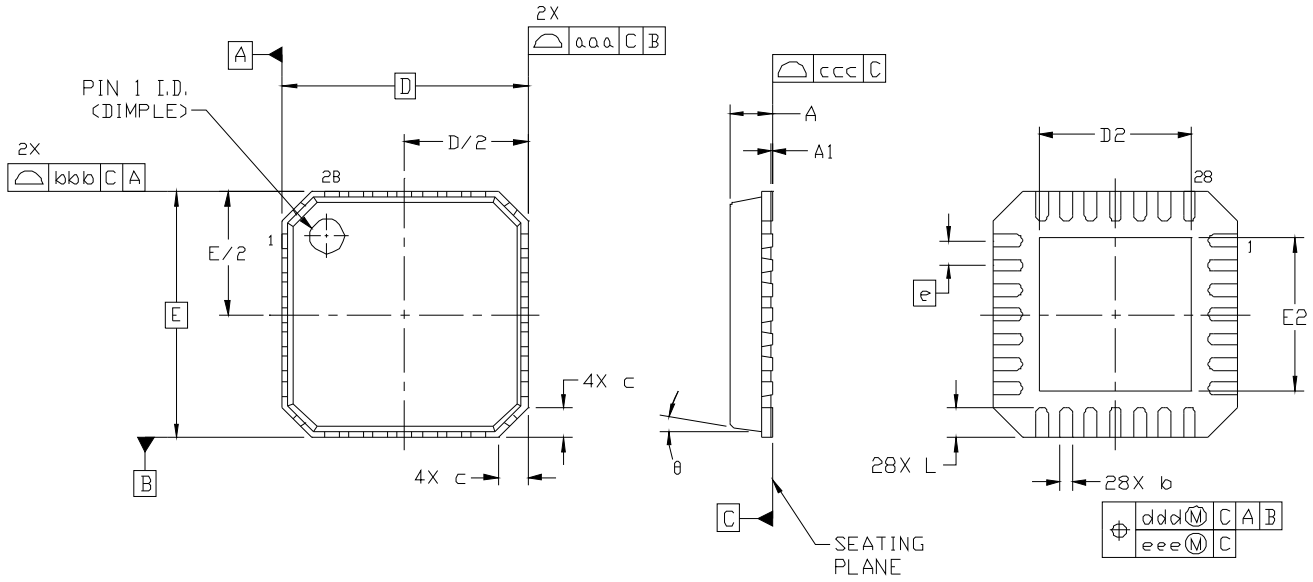


Figure 16. 28-Lead Quad Flat No-Lead (QFN)

Table 9. Package Diagram Dimensions

Controlling Dimension: mm

Symbol	Millimeters		
	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		5.00 BSC	
D2	2.95	3.10	3.25
e		0.50 BSC	
E		5.00 BSC	
E2	2.95	3.10	3.25
L	0.50	0.60	0.70
θ	0°	—	12°
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. 1.All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VHHD-1.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 1.0

- Added Figure 4, “PLL Acquisition Time,” on page 6.
- Table 2 on page 7
  - Added FEC (2.7 GHz) Supply Current
  - Updated values: Supply Current
  - Added FEC (2.7 GHz) Power Dissipation
  - Updated values: Power Dissipation
  - Updated values: Common Mode Input Voltage (REFCLK)
  - Updated values: Output Common Mode Voltage
- Table 3 on page 8
  - Added separate Output Clock Rise Time
  - Added separate Output Clock Fall Time
  - Updated values: Output Clock Rise Time
  - Updated values: Output Clock Fall Time
- Table 4 on page 9
  - Updated values: Jitter Tolerance (OC-48) for f = 1 MHz
  - Updated values: Acquisition Time (reference clock applied)
  - Updated values: Acquisition Time (reference-less operation)
  - Updated values: Freq Difference at which Receive PLL goes out of Lock
  - Updated values: Freq Difference at which Receive PLL goes into Lock
- Removed “Hysteresis Dependency” Figure.
- Added Figure 7, “LOS Signal Hysteresis,” on page 13.
- Corrected error: Table 8 on page 19—changed description for LOS_LVL from “LOS is disabled when the voltage applied is less than 500 mV” to “LOS is disabled when the voltage applied is less than 1.0 V.”

Revision 1.0 to Revision 1.1

- Corrected “Revision 0.1 to Revision 1.0” Change List.

Revision 1.1 to Revision 1.2

- Added Figure 5, “LOS Response Time,” on page 6.
- Updated Table 2 on page 7
  - Added “Output Common Mode Voltage (DOUT)” with updated values.
  - Added “Output Common Mode Voltage (CLKOUT)” with updated values.
- Table 3 on page 8.
  - Added “Output Clock Duty Cycle”
  - Added “Loss-of-Signal Response Time”
- Updated Table 8 on page 19
  - Changed “clock input” to “DIN inputs” for Loss-of-Signal.
- Updated Figure 16, “28-Lead Quad Flat No-Lead (QFN),” on page 23.
- Updated Table 9, “Package Diagram Dimensions,” on page 23.
  - Changed dimension A.
  - Changed dimension E2.

Revision 1.2 to Revision 1.3

- Table 2 on page 7.
  - Updated power consumption.
  - Updated R_{IN}.
- Table 3 on page 8.
  - Updated clock to data delay.
  - Updated slicing level accuracy.
- Table 4 on page 9.
  - Updated tolerance.
  - Updated acquisition time.
  - Updated reference clock information.
- Updated "6. Ordering Guide" on page 22.
  - Added “X” to part number.

Revision 1.3 to Revision 1.4

- Updated Table 2 on page 7.
  - Added limits for V_{ICM}.
  - Updated V_{OD}.
- Updated Table 3 on page 8.
  - Updated $T_{Cr\text{-}D}$.
  - Updated $T_{Cf\text{-}D}$.
  - Revised SLICE specification.
- Updated Table 4 on page 9.
  - T_{AQ} min/max values updated.
- Updated "4.7. Loss-of-Signal (LOS)" on page 13.
  - Added note describing valid signal.
  - Updated Figure 6, “LOS_LVL Mapping,” on page 13.
- Updated "4.9. Data Slicing Level" on page 14.
  - Added Figure 8 on page 14.
  - Revised text.

Revision 1.4 to Revision 1.5

- Added "7. Top Mark" on page 22.
- Updated "8. Package Outline" on page 23.

NOTES:

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